REMARKS

In the Office Action, the Examiner rejects claims 1-3, 6, 7, 16, 18, and 19 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,853,020 to Yu et al. ("Yu") and rejects claims 1-4, 6-13, 15, 16, 18 and 19 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication 2003/0151077 to Matthew et al. ("Matthew") in view of U.S. Patent No. 5,663,586 to Lin ("Lin").

By this Amendment, Applicants have canceled claims 8-13 and 15 without prejudice or disclaimer. Claims 1-4, 6, 7, 16, 18, and 19 remain pending.

The rejections of claims 8-13 and 15 under 35 U.S.C. § 103(a) are obviated by virtue of their cancellation.

Applicants respectfully traverse the claim rejections under 35 U.S.C. § 102(e) based on Yu. A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. See M.P.E.P. § 2131. Applicants submit that Yu does not teach every aspect of claims 1-3, 6, 7, 16, 18, and 19, either expressly or impliedly.

Claim 1 is directed to a semiconductor device comprising, among other things, a first sidewall spacer formed adjacent a first side of a fin, the first sidewall spacer having a substantially triangular shaped cross-section; a second sidewall spacer formed adjacent a second side of the fin, the second sidewall spacer having a substantially triangular shaped cross-section; and a gate formed over the fin and the first and second sidewall spacers, and in contact with the first and second sidewall spacers, in a channel region of the semiconductor device. The first and second sidewall spacers are formed to a width ranging from about 150 Å to about 1000 Å.

Yu does not disclose each of the features recited in claim 1. Yu does not disclose, for

instance, "a gate formed over the fin and the first and second sidewall spacers," as recited in claim 1. In contrast, Yu discloses a fin 210 having a dielectric cap 140. (Yu, Fig. 3 and column 4, lines 14 and 15). Spacers 410 and 420 are deposited around fin 210. (Yu, Fig. 4 and column 4, lines 16-27). Yu further discloses that a silicon gate material 710 is then deposited and planarized so that the gate material "is even with or nearly even with dielectric cap 140." (Yu, Figs. 7 and 8; and column 4 line 65 through column 4, line 13). The gate material 710 of Yu is clearly not formed over the fin, as is recited in claim 1. Instead, as is shown in Figs. 8 and 9A of Yu, gate material 710 is planarized so that it does not extend over fin 210. Extending gate material 710 over fin 210 would electrically couple gates 910 and 920 of Yu. In contradistinction, Yu discloses that "the gates are electrically and physically separated by fin 210." (Yu, column 5, lines 63-65).

For at least this reason, Applicants submit that Yu does not disclose each element of claim 1, and the rejection of this claim should therefore be withdrawn. At least by virtue of their dependency from claim 1, Applicants submit that the rejection of claims 2, 3, 6, and 7 based on Yu should also be withdrawn.

Claims 2, 3, 6, and 7 recite additional features that are not disclosed by Yu. Claim 2, for instance, states that the "the first and second sidewall spacers cause a topology of the gate to smoothly transition over the fin and the first and second sidewall spacers." Yu does not disclose this feature. Additionally, Applicants note that because Yu does discloses that gate material 710 is planarized such that it is not formed over fin 210, Yu could not possibly disclose a smooth transition of the gate material "over the fin and the first and second sidewall spacers," as recited in claim 1 (emphasis added).

Claims 16, 18, and 19 additionally stand rejected under 35 U.S.C. § 102(e) based on Yu.

Claim 16 is directed to a FinFET device comprising a number of features, including, for example, a gate material layer formed over a fin, a first sidewall spacer, and a second sidewall spacer, and in contact with the first and second sidewall spacers, in a direction perpendicular to a direction of the fin, whereby the first and second sidewall spacers cause a topology of the gate material layer to smoothly transition over the fin and the first and second sidewall spacers.

As with claim 1, Yu does not disclose each of the features of the FinFET device recited in claim 16. Yu, for example, does not disclose "a gate material layer formed over a fin," as recited in claim 16. As previously discussed, gates 910 and 920 of Yu are specifically disclosed as being planarized so that they are not over fin 210. Thus, Yu does not disclose this feature of claim 16.

Claim 16 additionally recites that the first and second sidewall spacers are formed in a "roughly triangular shape" and the gate material is formed over the sidewall spacers "whereby the first and second sidewall spacers cause a topology of the gate material layer to smoothly transition over the fin and the first and second sidewall spacers." As mentioned above, Yu does not even disclose that a topology of the gate smoothly transitions over a fin and the first and second sidewall spacers, and thus, could not possibly disclose or suggest this feature of claim 16.

For at least these reasons, Applicants submit that Yu does not disclose each element of claim 16, and the rejection of this claim based on Yu should therefore be withdrawn. At least by virtue of their dependency from claim 16, Applicants submit that the rejections of claims 18 and 19 based on Yu should also be withdrawn.

Claims 1-4, 6, 7, 16, 18, and 19 stand rejected under 35 U.S.C. § 103(a) based on Mathew in view of Lin. In rejecting independent claims 1, 8, and 16 based on Mathew and Lin, the Examiner contends that Mathew discloses most of the features of these claims, but concedes

that Mathew does not disclose sidewall spacers having the width recited in these claims. (Office Action, pages 5, 7, and 9). The Examiner contends, however, that Lin discloses sidewall spacers having the claimed width and that one of ordinary skill in the art would have found it obvious to combine Mathew and Lin.

Applicants respectfully disagree with the Examiner's interpretation of Mathew. In particular, Applicants submit that Mathew discloses planarizing a gate material layer to form separate gate electrodes that cannot be said to be formed "over the fin," as recited in claim 1. (Mathew, Abstract). More specifically, as shown in Fig. 15, Mathew discloses a silicon layer 18 (which the Examiner contends corresponds to the fin recited in claim 1) surrounded by polysilicon regions 62' and 64' (which the Examiner contends corresponds to the first and second sidewall spacers recited in claim 1) and first and second gates 46 and 48. (see Mathew, Fig. 15 and paragraph 30). Gates 46 and 48, however, are clearly shown in Fig. 15 as not extending over region 18. Instead, they are specifically disclosed in Mathew as being either etched or chemically mechanically polished to obtain the separate first and second gates 46 and 46. (Matthew, paragraph 30). Accordingly, Mathew does not disclose "a gate formed over the fin and the first and second sidewall spacers," as is recited in claim 1.

In rejecting claim 1, the Examiner appears to contend that in some figures, such as Fig. 14, Mathew discloses a gate 66 that is formed over silicon layer 18. Applicants note that although gate 66 is shown as a single layer in Fig. 14 of Mathew, the structure of Fig. 14 does not represent a final semiconductor device. Rather, Fig. 14 merely shows an intermediate processing step before gate 66 is planarized and formed into the first and second gates. One of ordinary skill in the art reading Mathew in its entirety would not interpret Mathew to disclose a device in which gate 66 is left to extend over silicon layer 18.

Applicants have reviewed Lin, and submit that Lin also fails to remedy the deficiencies of Mathew with respect to claim 1.

For at least these reasons, Applicants submit that Mathew and Lin, either alone or in combination, do not disclose or suggest each feature of claim 1.

Additionally, Applicants submit that the Examiner has not shown proper motivation to combine Mathew and Lin in the manner suggested. The Examiner relies on Lin for the width of the sidewall spacers recited in claim 1, and states that "[I]t would have been obvious to one skilled in this art to form Mathew's polysilicon sidewall spacers with a width of about 150 Å to about 1000 Å because Lin teaches that polysilicon sidewall spacers are conventionally formed that thick." (Office Action, page 5). Applicants respectfully disagree with the Examiner's conclusion of obviousness. Mathew discloses a vertical double gate semiconductor device in which a silicon fin layer extends vertically from the substrate of the device. Lin discloses a more conventional FET device. (Lin, See Title and Abstract). Applicants submit that these two structures would be recognized by one of ordinary skill in the art as different types of semiconductor FET structures and that specific parameters (such as the width of a spacer) in one device could not simply be applied to the other device. Accordingly, one of ordinary skill in the art reading Lin would not be motivated to use the spacer width disclosed by Lin as the width of the floating gate disclosed by Mathew. Thus, Applicants submit that the Examiner has not made a *prima facie* case of obviousness with regard to Mathew and Lin.

For at least these reasons, Applicants submit that the rejection of claim 1 under 35 U.S.C. § 103(a) based on Mathew and Lin is improper and should be withdrawn. At least by virtue of their dependency on claim 1, the rejections of claims 2, 3, 4, 6, and 7 based on Mathew and Lin is also improper and should be withdrawn.

Claims 2, 3, 4, 6, and 7 recite additional features that are not disclosed by Mathew and Lin, either alone or in combination. Claim 2, for instance, states that the "the first and second sidewall spacers cause a topology of the gate to smoothly transition over the fin and the first and second sidewall spacers." Mathew does not disclose this feature and indeed, does not even discuss the desirability of causing a topology of the gate to smoothly transition over the fin and the first and second sidewall spacers. Additionally, Applicants note that because Mathew discloses that gate material 66 is planarized to create first and second gates that are not formed over silicon layer 18, Mathew could not possibly disclose a smooth transition of the gate material "over the fin and the first and second sidewall spacers," as recited in claim 2 (emphasis added).

Claims 16, 18, and 19 additionally stand rejected under 35 U.S.C. § 103(a) based on Mathew and Lin. Applicants respectfully traverse this rejection.

As with claim 16, Mathew does not disclose each of the features of the FinFET device recited in claim 16. Mathew, for example, does not disclose "a gate material layer formed over a fin," as recited in claim 16. As previously discussed, gate layer 66 of Mathew is specifically disclosed as being planarized to form first and second gates that are clearly shown as not protruding over silicon layer 18. Thus, contrary to the Examiner's assertions, Mathew does not disclose this feature of claim 16.

Claim 16 additionally recites that the first and second sidewall spacers are formed in a "roughly triangular shape" and the gate material is formed over the sidewall spacers "whereby the first and second sidewall spacers cause a topology of the gate material layer to smoothly transition over the fin and the first and second sidewall spacers." As mentioned above, Mathew does not even discuss the desirability of causing a topology of the gate to smoothly transition over a fin and the first and second sidewall spacers, and thus, could not possibly disclose or

suggest this feature of claim 16.

In rejecting claim 16, the Examiner relies on Lin for disclosure relating to the claimed width of the sidewall spacers. Applicants submit that Lin does not cure the above-noted deficiencies of Mathew.

For at least these reasons, Applicants submit that Mathew and Lin, either alone or in combination, do not disclose or suggest each feature of claim 16.

Additionally, for reasons similar to those given above with respect to claim 1, Applicants submit that the Examiner has not made a *prima facie* case of obviousness with regard to Mathew and Lin. That is, Mathew discloses a vertical double gate semiconductor device and Lin discloses a more conventional FET device. These two structures would be recognized by one of ordinary skill in the art as different types of semiconductor FET structures and that specific parameters (such as the width of a spacer) in one device could not simply be applied to the other device. Thus, Applicants submit that the Examiner has not made a *prima facie* case of obviousness with regard to Mathew and Lin.

For at least these reasons, Applicants submit that the rejection of claim 16 under 35 U.S.C. § 103(a) based on Mathew and Lin is improper and should be withdrawn. At least by virtue of their dependency on claim 16, the rejection of claims 18 and 19 based on Mathew and Lin are also improper and should be withdrawn.

In view of the foregoing amendments and remarks, Applicants submit that the claimed invention is neither anticipated nor rendered obvious in view of the prior art references cited against this application. Applicants therefore request the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is

hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: August 17, 2005

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